**Fig. 1A**

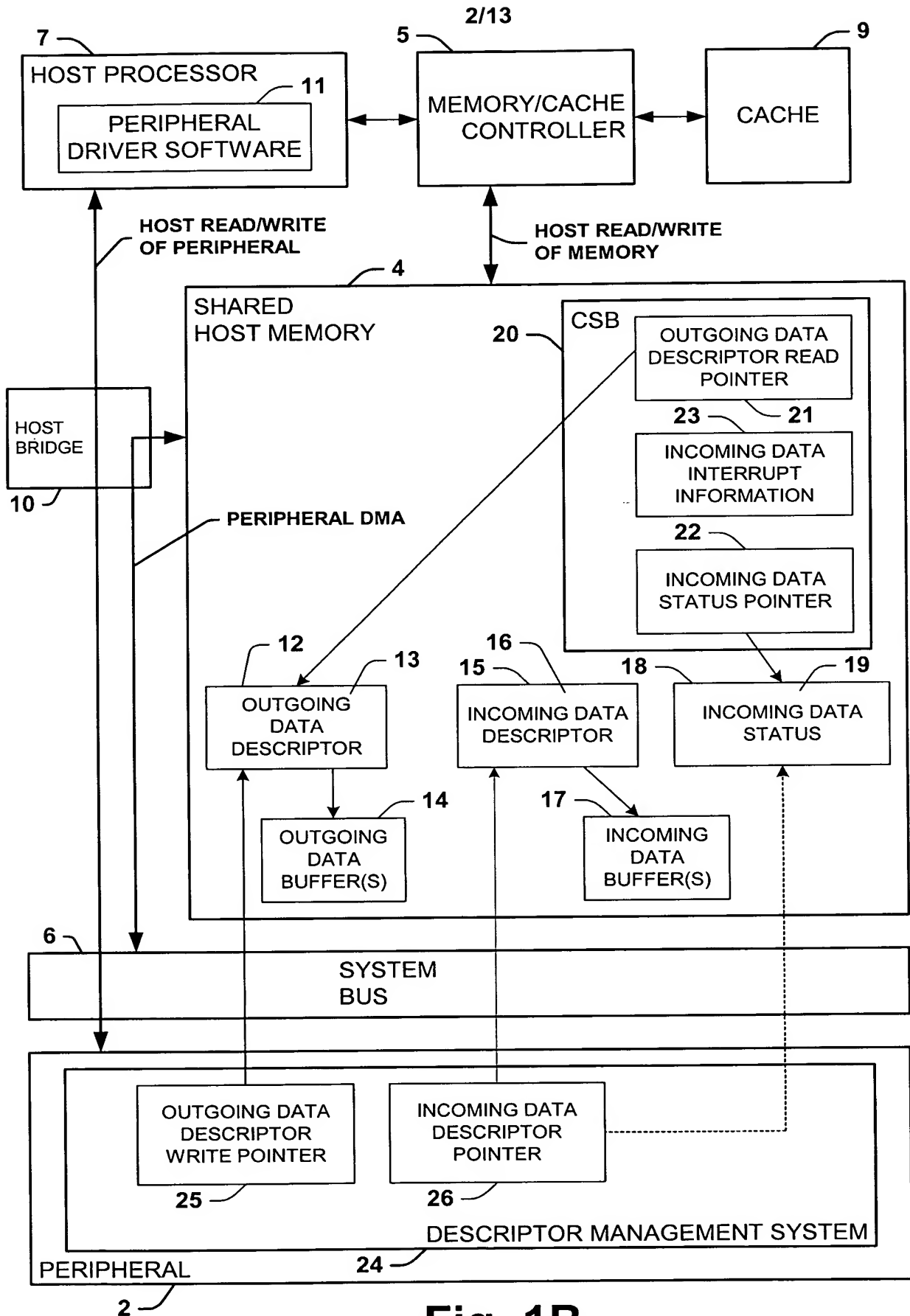
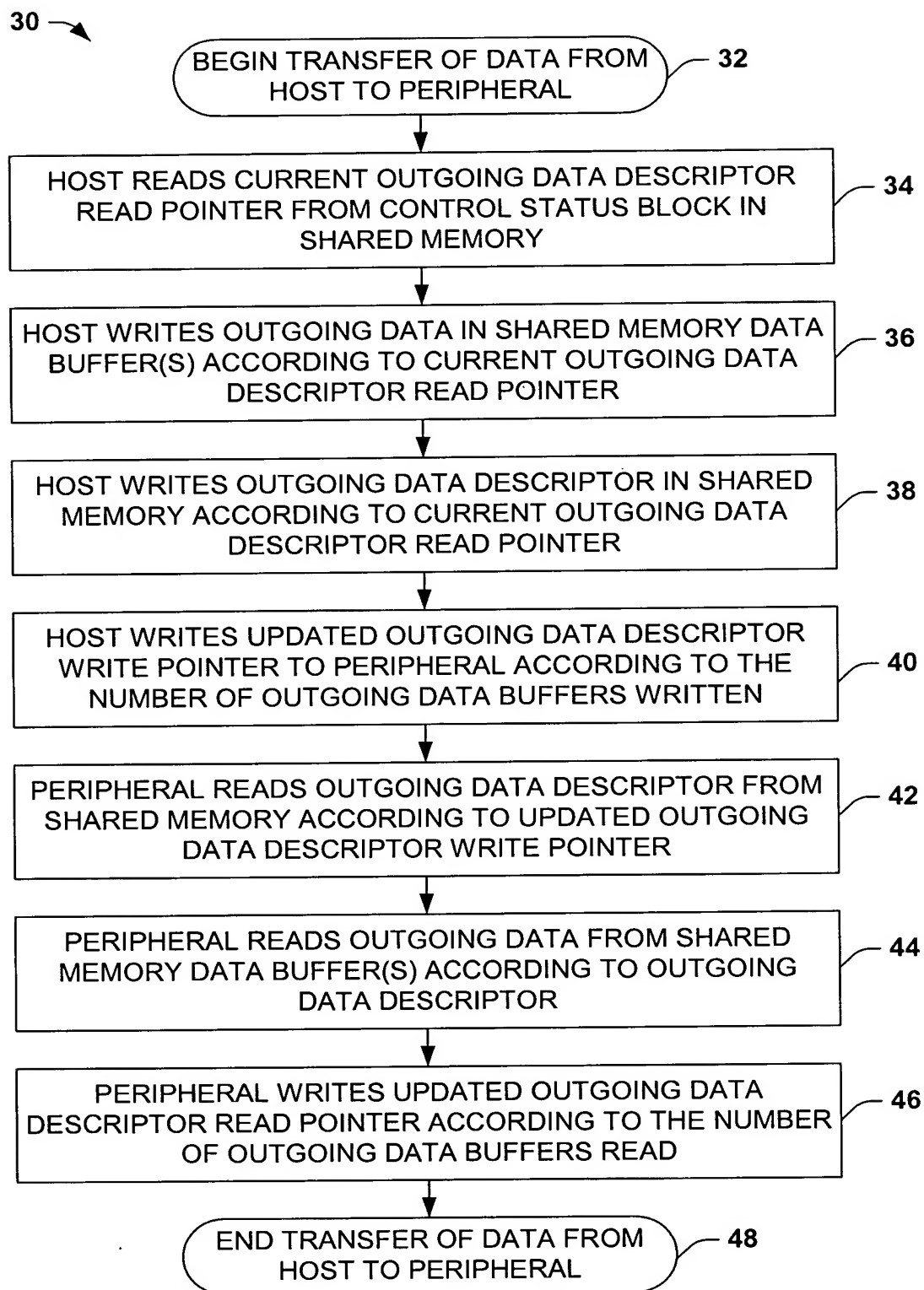
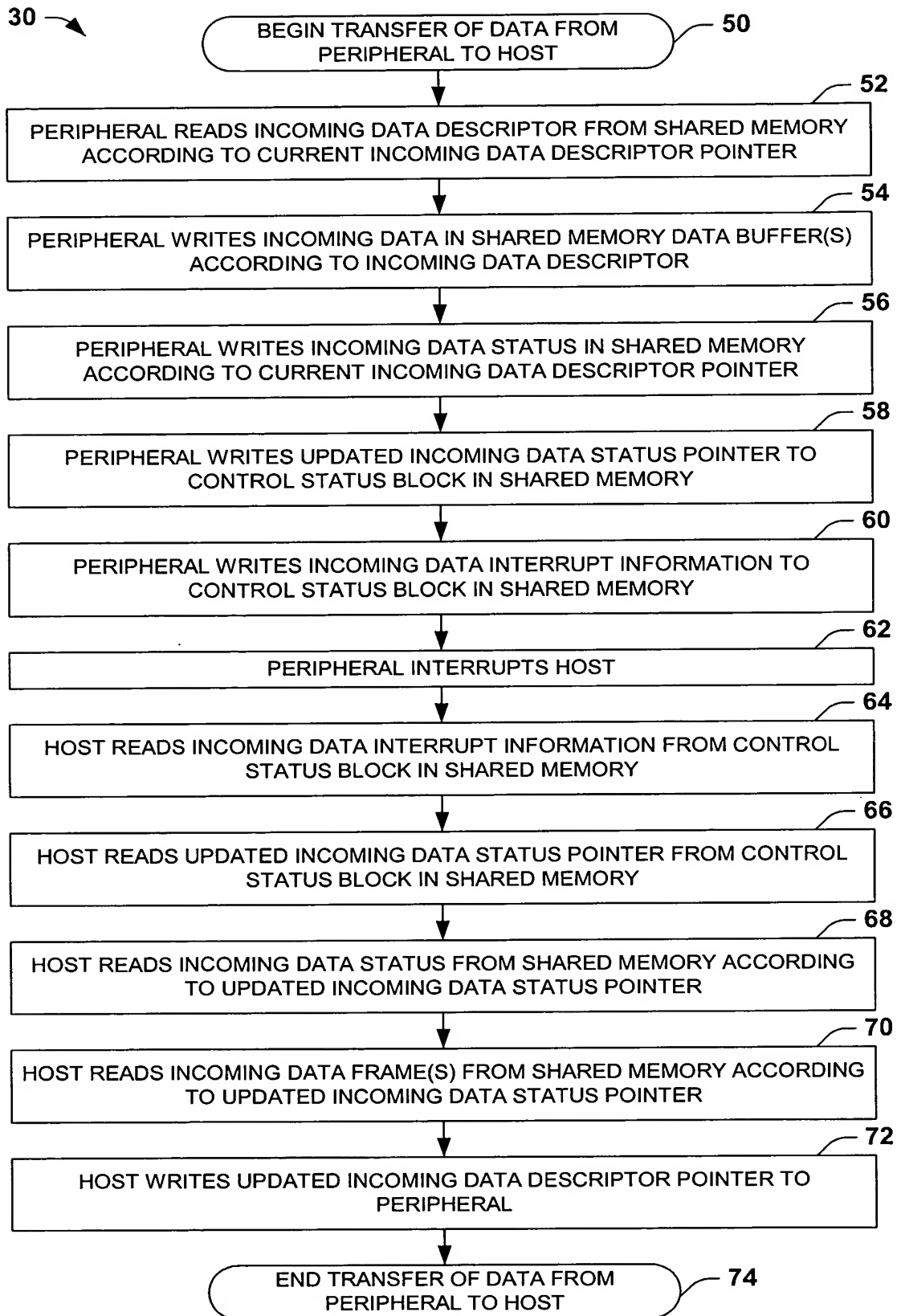


Fig. 1B

**Fig. 1C**

**Fig. 1D**

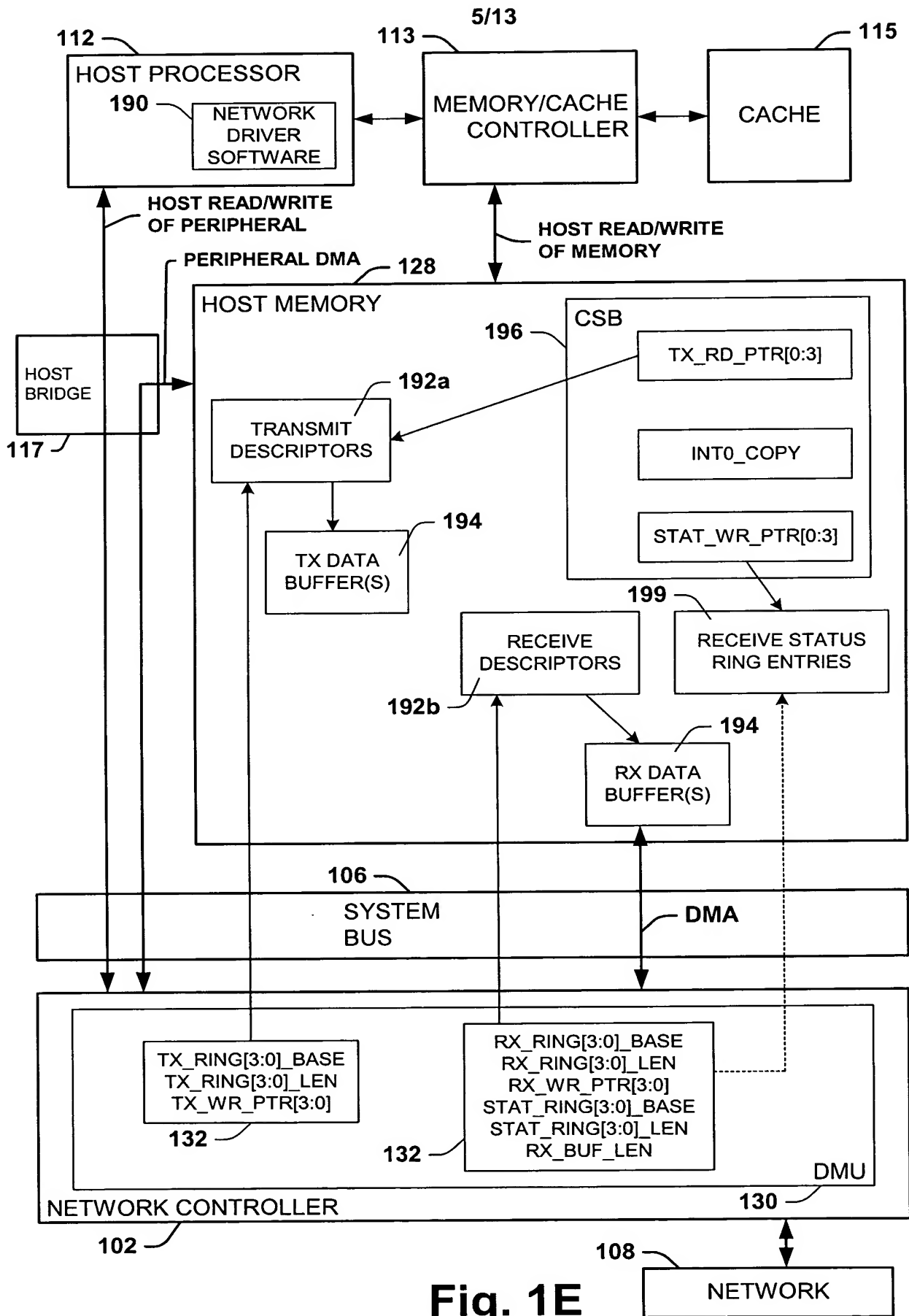


Fig. 1E

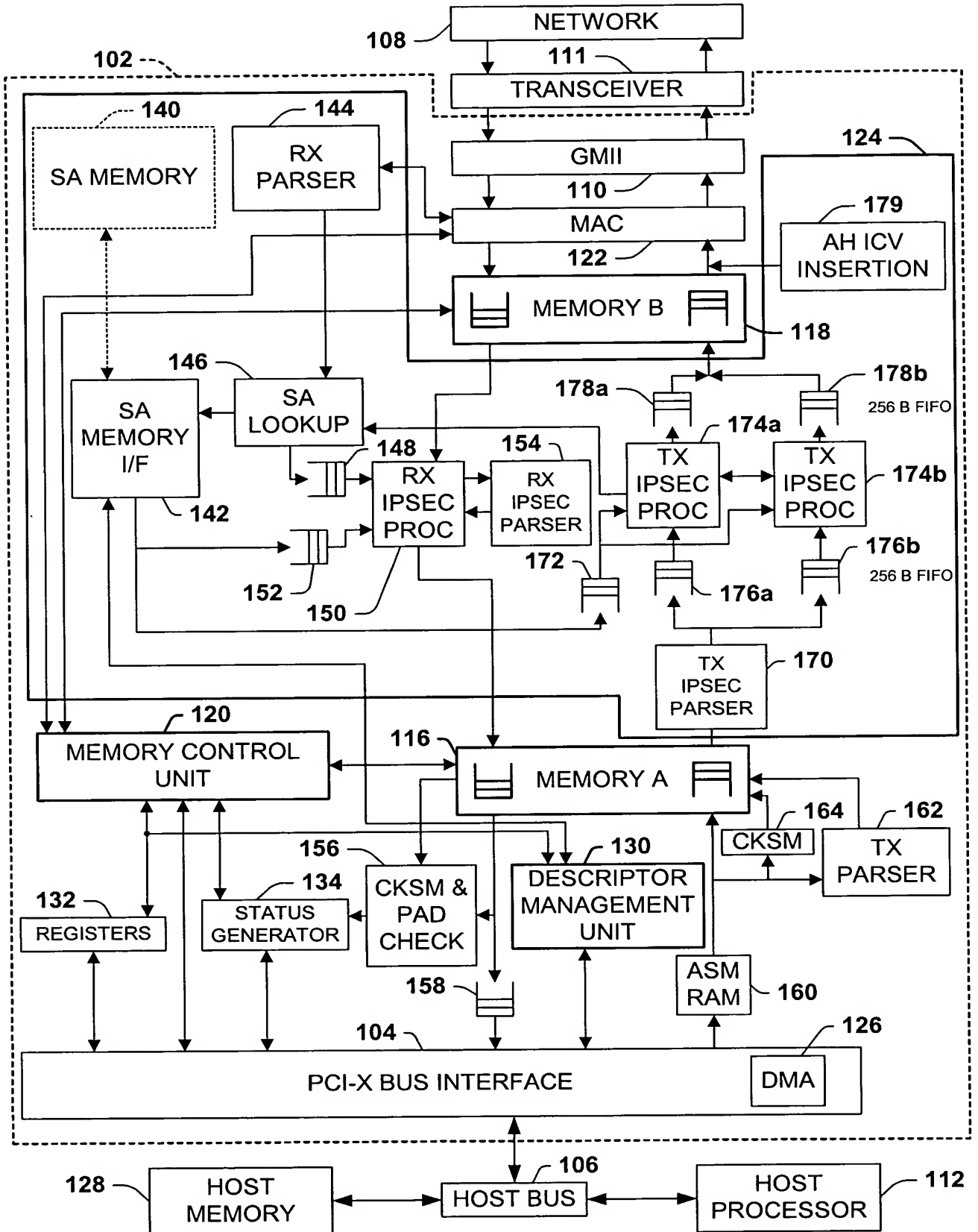


Fig. 2

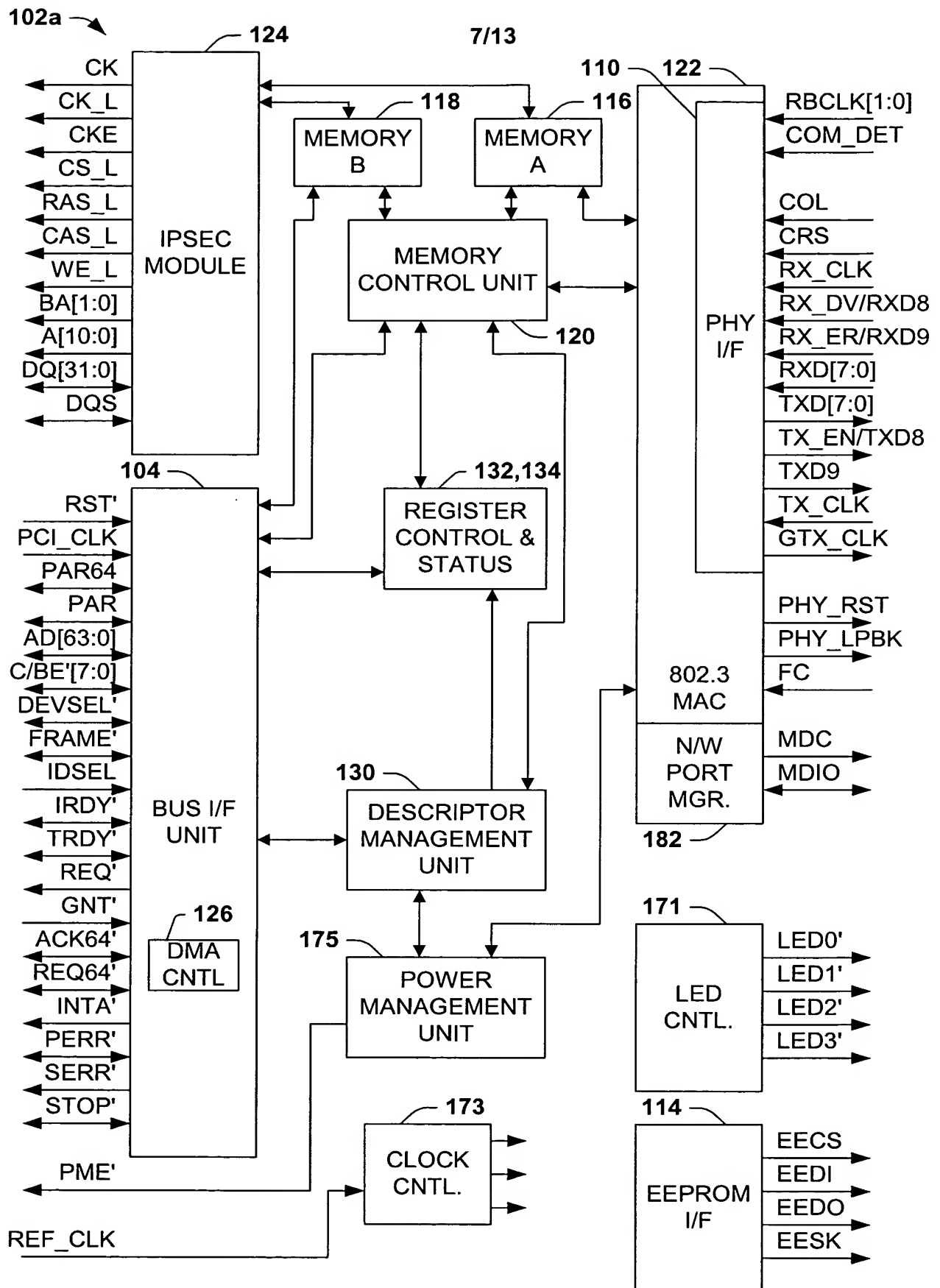
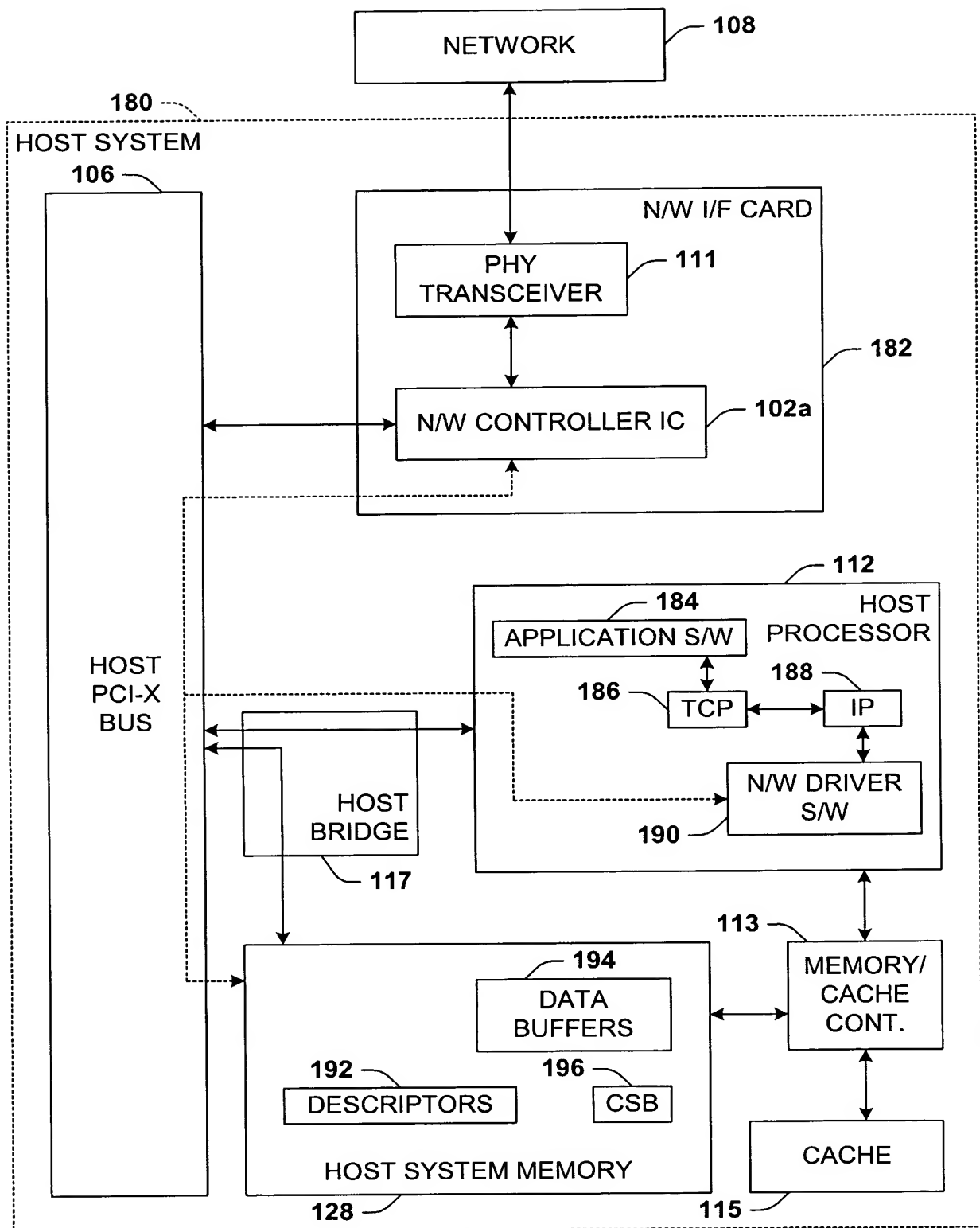


Fig. 3

**Fig. 4**

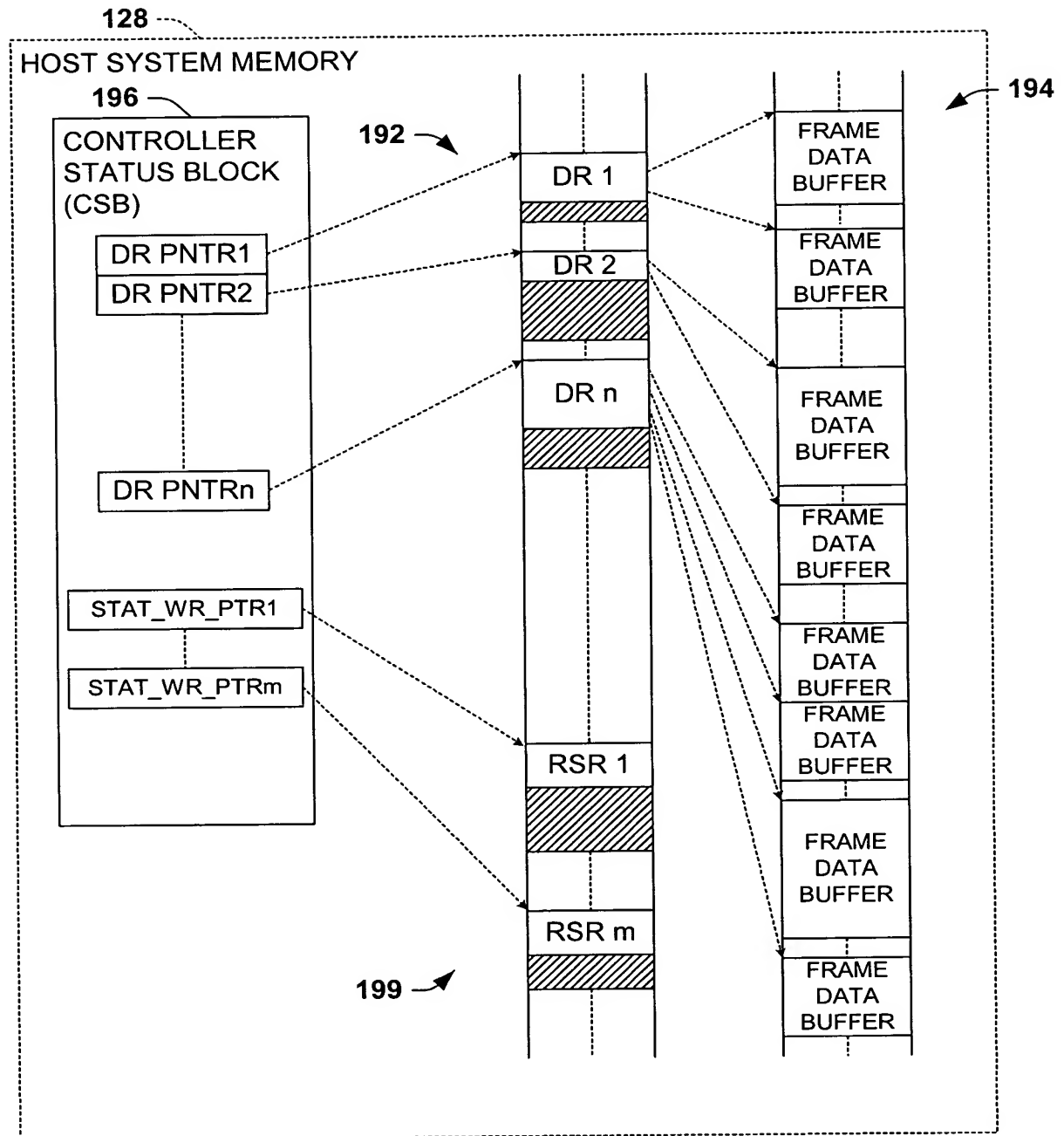


Fig. 5A

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CSB

TX_RD_PTR0
TX_RD_PTR1
TX_RD_PTR2
TX_RD_PTR3
STAT_WR_PTR0
STAT_WR_PTR1
STAT_WR_PTR2
STAT_WR_PTR3
INT0_COPY

Fig. 5B

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REGISTERS

RX_RING[3:0]_BASE
TX_RING[3:0]_BASE
RX_RING[3:0]_LEN
TX_RING[3:0]_LEN
TX_WR_PTR[3:0]
RX_WR_PTR[3:0]
STAT_RING[3:0]_BASE
STAT_RING[3:0]_LEN
RX_BUF_LEN
CSB_ADDR

Fig. 5C

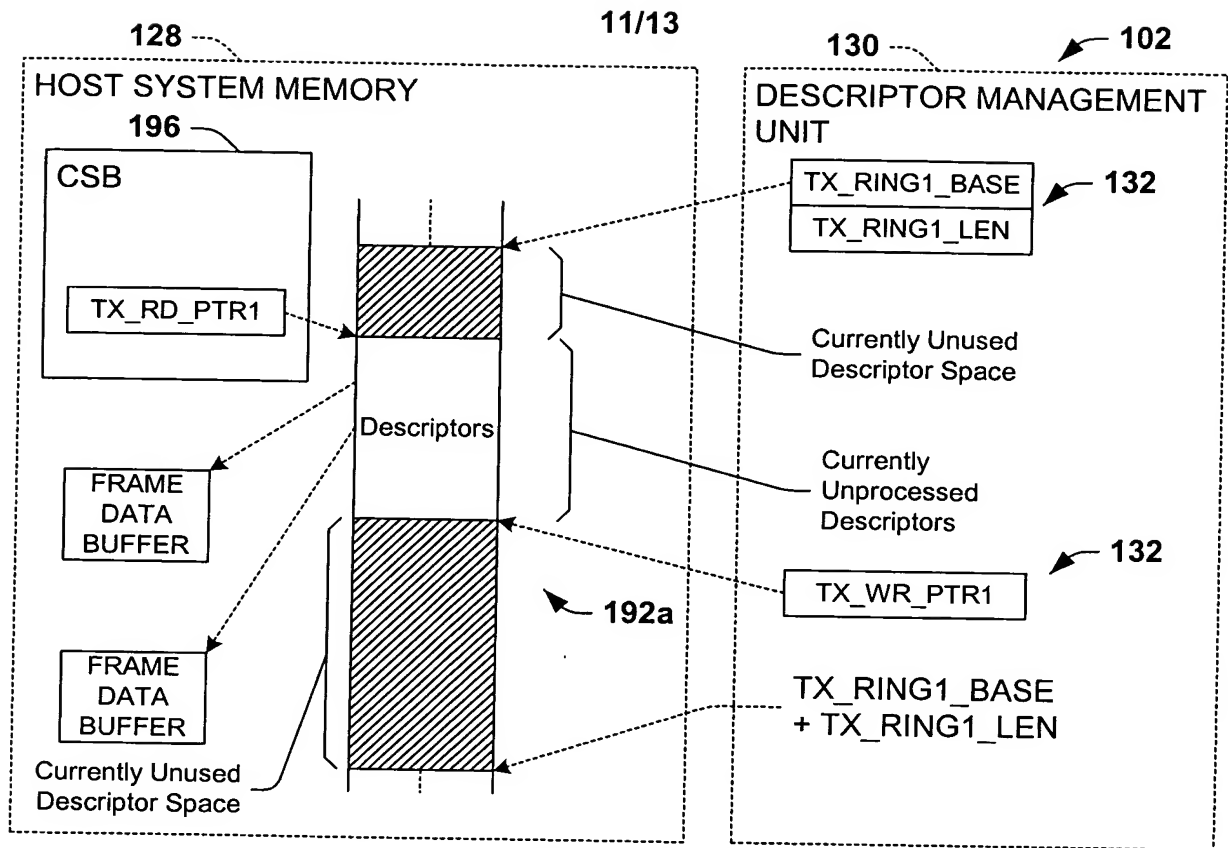


Fig. 5D

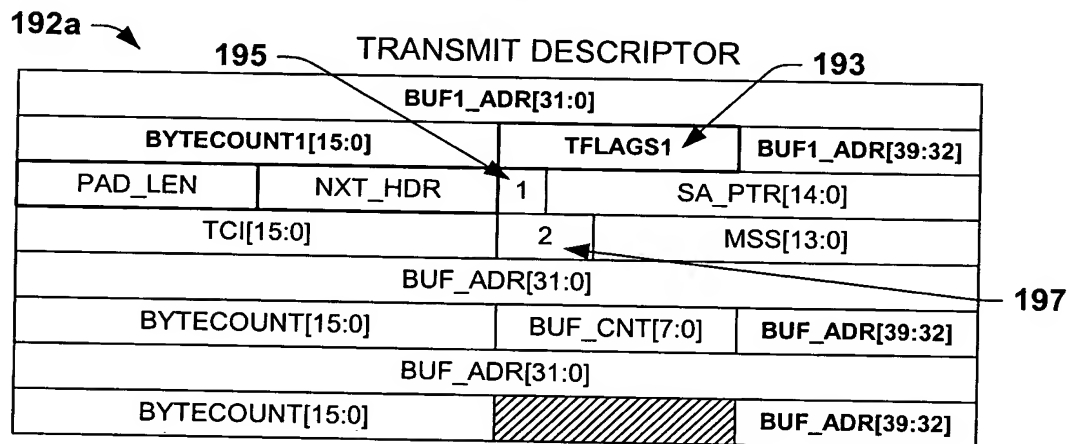


Fig. 5E

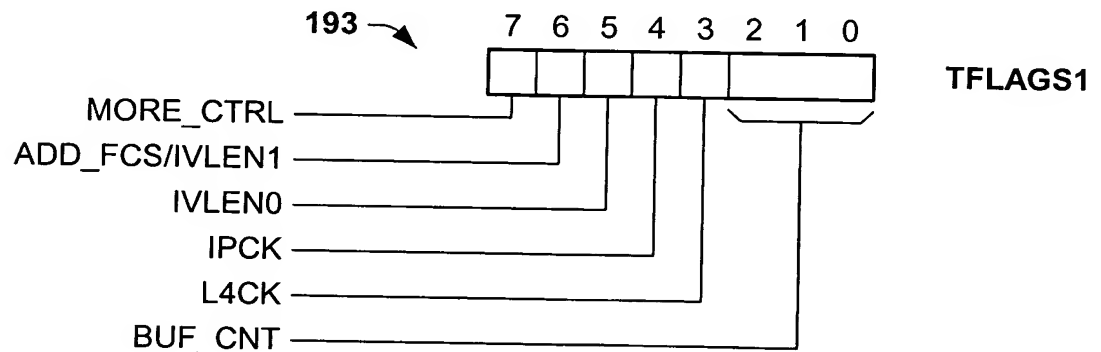


Fig. 5F

192b

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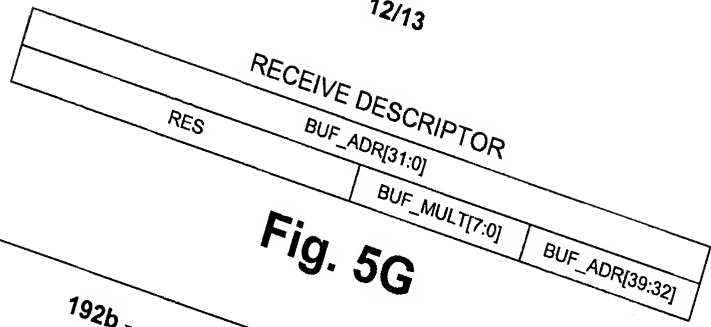


Fig. 5G

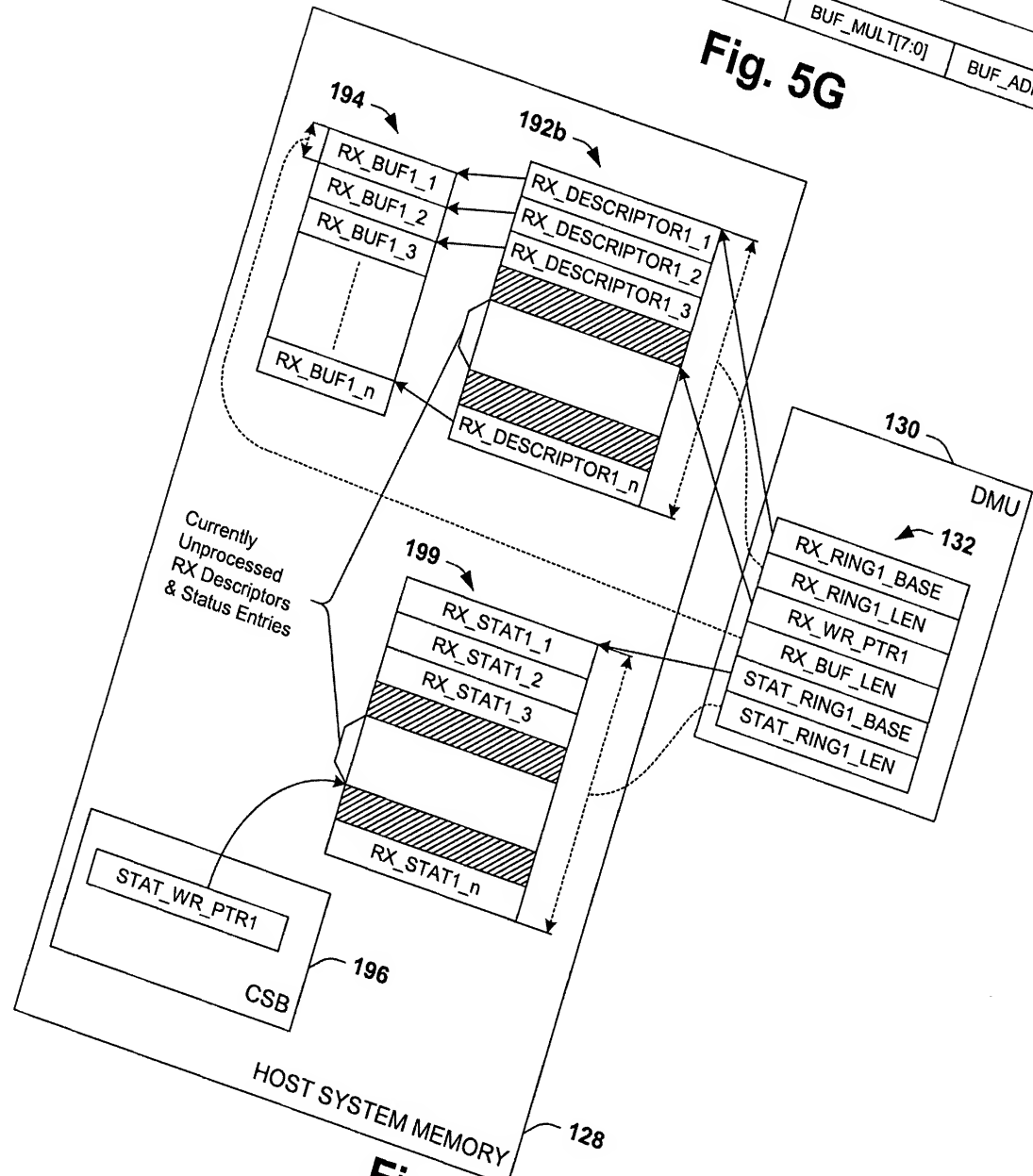
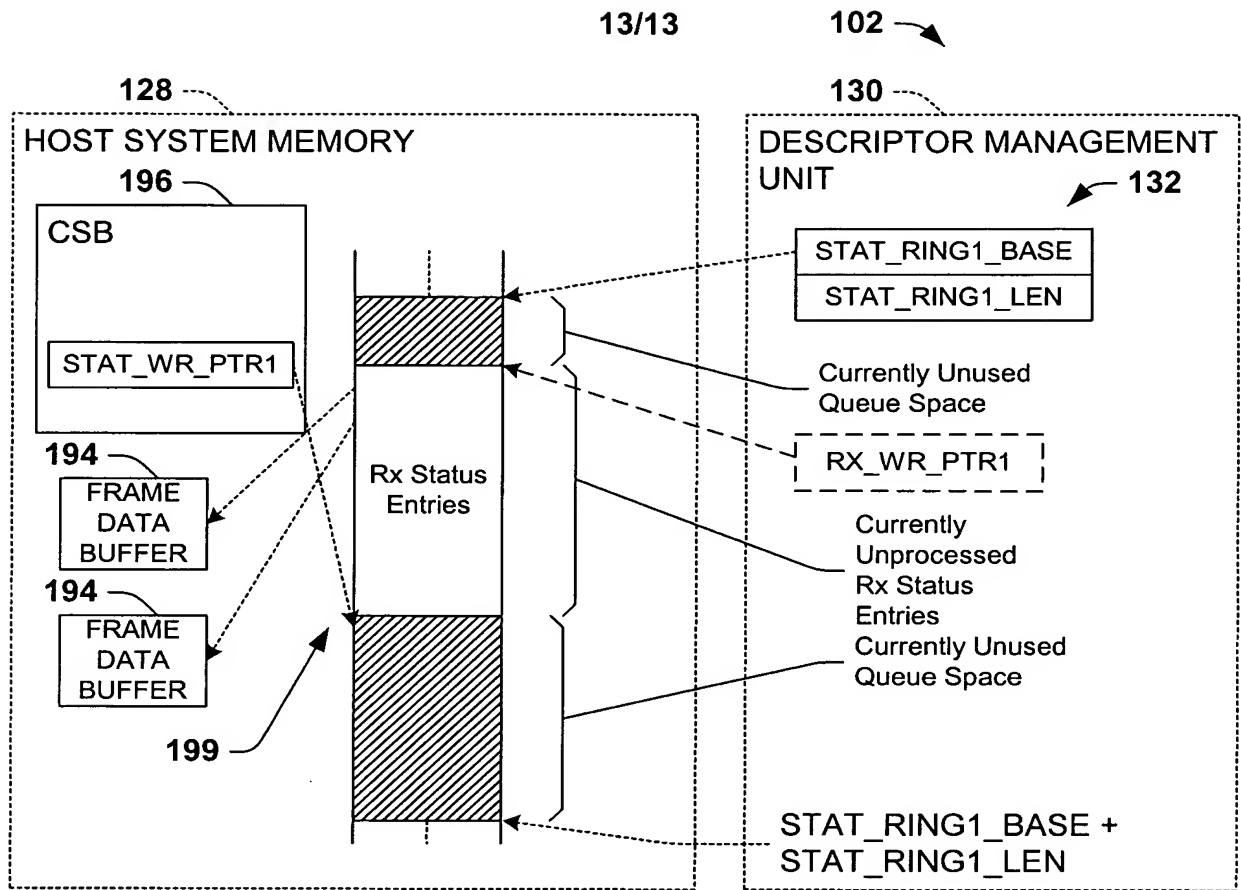
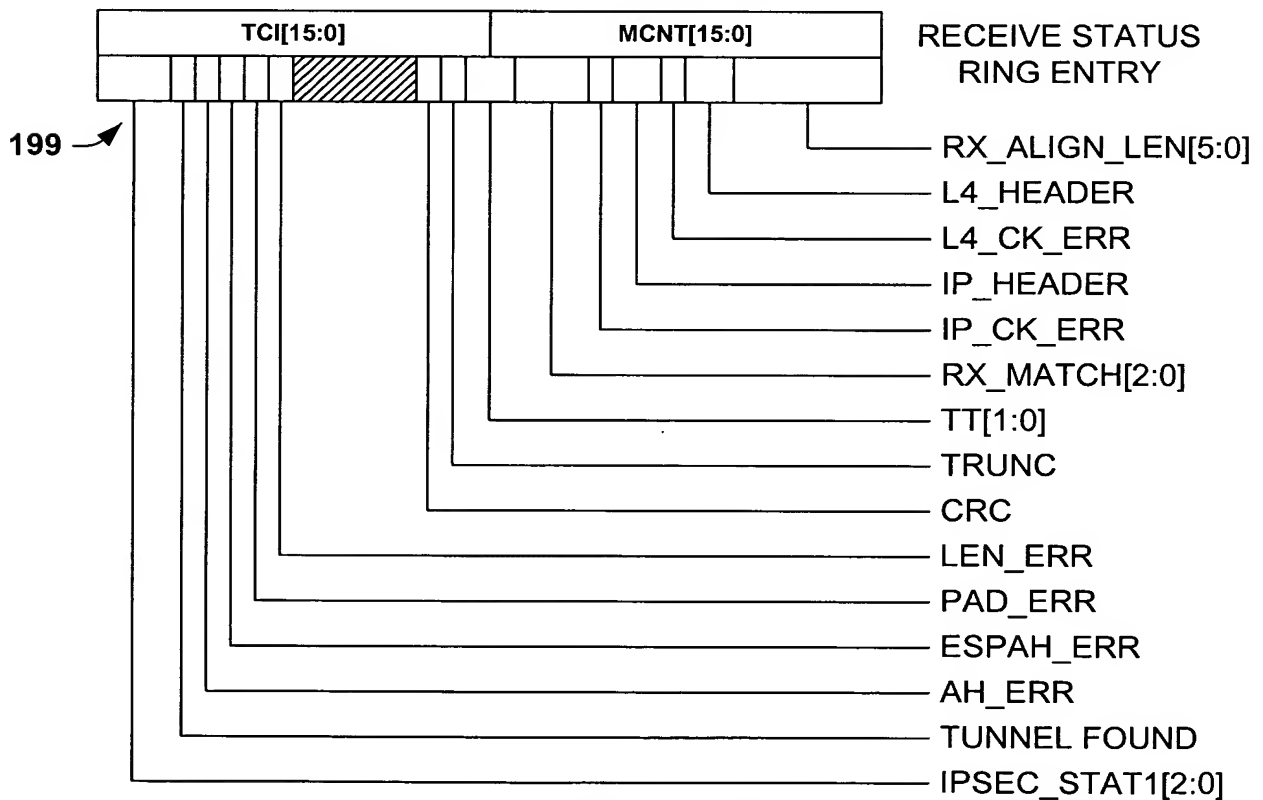


Fig. 5H

**Fig. 5I****Fig. 5J**